

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 1. (Currently amended) A method for achieving low gate leakage current
2 in an integrated circuit during sleep mode, comprising reducing a power supply
3 voltage applied to the integrated circuit to a low voltage level upon entering sleep
4 mode, wherein the low voltage level is low enough to achieve low gate leakage
5 current, but is high enough to maintain state in the integrated circuit, and wherein
6 reducing the power supply voltage involves stepping the power supply voltage in
7 discrete steps to the low voltage level to reduce noise caused by the voltage
8 change.

1 2. (Original) The method of claim 1, wherein the low voltage level is so
2 low that the integrated circuit cannot perform computation operations on data.

1 3. (Original) The method of claim 1, wherein the low voltage level is
2 below a threshold voltage for transistors on the integrated circuit.

1 4. (Original) The method of claim 1, further comprising restoring the
2 power supply voltage to a nominal operating voltage upon detecting that sleep
3 mode is about to be exited.

1 5. (Original) The method of claim 4, wherein reducing the power supply
2 voltage involves gradually ramping the power supply voltage to the low voltage
3 level to reduce noise caused by the voltage change.

1 6. (Original) The method of claim 4, wherein restoring the power supply
2 voltage involves gradually ramping the power supply voltage to the nominal
3 operating voltage to reduce noise caused by the voltage change.

1 7 (Canceled).

1 8. (Original) The method of claim 4, wherein restoring the power supply
2 voltage involves stepping the power supply voltage in discrete steps to the
3 nominal operating voltage to reduce noise caused by the voltage change.

1 9. (Original) The method of claim 1, wherein the low voltage level is also
2 low enough to provide a low subthreshold leakage current in the integrated circuit.

1 10. (Currently amended) An apparatus for achieving low gate leakage
2 current in an integrated circuit during sleep mode, comprising a reducing
3 mechanism configured to reduce a power supply voltage applied to the integrated
4 circuit to a low voltage level upon entering sleep mode, wherein the low voltage
5 level is low enough to achieve low gate leakage current, but is high enough to
6 maintain state in the integrated circuit, and reducing the power supply voltage
7 involves stepping the power supply voltage in discrete steps to the low voltage
8 level to reduce noise caused by the voltage change.

1 11. (Original) The apparatus of claim 10, wherein the low voltage level is
2 so low that the integrated circuit cannot perform computation operations on data.

1 12. (Original) The apparatus of claim 10, wherein the low voltage level is
2 below a threshold voltage for transistors on the integrated circuit.

1 13. (Original) The apparatus of claim 10, further comprising a restoring
2 mechanism configured to restore the power supply voltage to a nominal operating
3 voltage upon detecting that sleep mode is about to be exited.

1 14. (Original) The apparatus of claim 13, wherein reducing the power
2 supply voltage involves gradually ramping the power supply voltage to the low
3 voltage level to reduce noise caused by the voltage change.

1 15. (Original) The apparatus of claim 13, wherein restoring the power
2 supply voltage involves gradually ramping the power supply voltage to the
3 nominal operating voltage to reduce noise caused by the voltage change.

1 16 (Canceled).

1 17. (Original) The apparatus of claim 13, wherein restoring the power
2 supply voltage involves stepping the power supply voltage in discrete steps to the
3 nominal operating voltage to reduce noise caused by the voltage change.

1 18. (Original) The apparatus of claim 10, wherein the low voltage level is
2 also low enough to provide a low subthreshold leakage current in the integrated
3 circuit.

1 19. (Currently amended) An integrated circuit that achieves low gate
2 leakage current during sleep mode, comprising a reducing mechanism configured
3 to reduce a power supply voltage applied to the integrated circuit to a low voltage

4 level upon entering sleep mode, wherein the low voltage level is low enough to
5 achieve low gate leakage current, but is high enough to maintain state in the
6 integrated circuit, and wherein reducing the power supply voltage involves
7 stepping the power supply voltage in discrete steps to the low voltage level to
8 reduce noise caused by the voltage change.

1 20. (Original) The integrated circuit of claim 19, wherein the low voltage
2 level is so low that the integrated circuit cannot perform computation operations
3 on data.

1 21. (Original) The integrated circuit of claim 19, wherein the low voltage
2 level is below a threshold voltage for transistors on the integrated circuit.

1 22. (Original) The integrated circuit of claim 19, further comprising a
2 restoring mechanism configured to restore the power supply voltage to a nominal
3 operating voltage upon detecting that sleep mode is about to be exited.

1 23. (Original) The integrated circuit of claim 22, wherein reducing the
2 power supply voltage involves gradually ramping the power supply voltage to the
3 low voltage level to reduce noise caused by the voltage change.

1 24. (Original) The integrated circuit of claim 22, wherein restoring the
2 power supply voltage involves gradually ramping the power supply voltage to the
3 nominal operating voltage to reduce noise caused by the voltage change.

1 25 (Canceled).

1 26. (Original) The integrated circuit of claim 22, wherein restoring the
2 power supply voltage involves stepping the power supply voltage in discrete steps
3 to the nominal operating voltage to reduce noise caused by the voltage change.

1 27. (Original) The integrated circuit of claim 19, wherein the low voltage
2 level is also low enough to provide a low subthreshold leakage current in the
3 integrated circuit.